IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Robert A. Shearer	§	Confirmation No.: 8448
	§	
	§	Group Art Unit: 2188
Serial No.: 10/677,425	§	
	§	Examiner: Craig E. Walter
Filed: 10/2/03	§	
	§	
For: SHARED BUFFER HAVING HARDWARE CONTROLLED BUFFER REGIONS	§	

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office to fax number 571-273-8300 to the attention of Examiner Craig E. Walter, or electronically filed, on the date shown below:

May 31, 2006
Date

Randol W. Read

RESPONSE TO OFFICE ACTION DATED MARCH 9, 2006

In response to the Office Action dated March 9, 2006, having a shortened statutory period for response set to expire on June 9, 2006, please enter this response and reconsider the claims pending in the application for reasons discussed below. While no fees are believed due, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 09-0465/ROC920030170US1 for any fees, including extension of time fees or excess claim fees, required to make this response timely and acceptable to the Office.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper. Amendments to the Drawings begin on page 6 of this paper and include both an attached replacement sheet and an annotated sheet showing changes. Remarks/Arguments begin on page 7 of this paper.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A memory device, comprising:

a buffer memory having a plurality of addressable memory registers;

a counter having a plurality of storage registers;

a logic network for writing and reading data into and out of said buffer memory, said logic network for partitioning said buffer memory into a plurality of buffer regions, wherein said logic network writes and reads data from a plurality of data classes into said plurality of buffer regions such that each data class is written into and read from a different buffer region, and wherein said logic network increments a storage register associated with a buffer region each time that buffer region reaches a predetermined usage level; and

a timer for periodically sending a timing signal to said logic network;

wherein in response to said timing signal said logic network recalls data from said counter registers and re-partitions said buffer memory such that a more utilized buffer region is assigned more addressable memory registers.

2. (Original) A memory device according to claim 1 wherein said logic network assigns a buffer region that is used less often fewer addressable memory registers.

3. (Original) A memory device according to claim 1 wherein each buffer region is always assigned at least a minimum number of addressable memory registers.

4. (Original) A memory device according to claim 1 wherein said predetermined usage level is full.

5. (Currently Amended) A memory device according to claim 1 wherein when ~~the~~ a least used buffer region is assigned ~~the~~ a minimum number of addressable memory registers the logic network assigns a buffer region that is less often fully utilized but that has more than the minimum number of addressable memory registers.

6. (Original) A memory device according to claim 1 wherein said data classes represent virtual lanes.

7. (Currently Amended) A memory device according to claim 1 wherein said timing signal initiates ~~are reset~~ clearing of said plurality of storage registers.

8. (Currently Amended) A switch network comprising:

a network switch;

a card adaptor for transmitting and receiving data from said network switch, and

a memory device for storing data for and from said card adaptor, said memory having:

a buffer memory having a plurality of addressable memory registers;

a counter having a plurality of storage registers;

a logic network for writing and reading data into and out of said buffer memory, said logic network for partitioning said buffer memory into a plurality of buffer regions, wherein said logic network writes and reads data from a plurality of data classes into said plurality of buffer regions such that each data class is written into and read from a different buffer region, and wherein said logic network increments a storage register associated with a buffer region each time that buffer region reaches a predetermined usage level; and

a timer for periodically sending a timing signal to said logic network;

wherein in response to said timing signal said logic network recalls data from said counter registers and re-partitions said buffer memory such that a more utilized buffer region is assigned more addressable memory registers.

9. (Original) A switch network according to claim 8 wherein said logic network assigns a buffer region that is used less often fewer addressable memory registers.

10. (Original) A switch network according to claim 8 wherein each buffer region is always assigned at least a minimum number of addressable memory registers.

11. (Original) A switch network according to claim 8 wherein said predetermined usage level is full.

12. (Currently Amended) A switch network according to claim 8 wherein when ~~the~~ a least used buffer region is assigned ~~the~~ a minimum number of addressable memory registers the logic network assigns a buffer region that is less often fully utilized but that has more than the minimum number of addressable memory registers.

13. (Original) A switch network according to claim 8 wherein said data classes represent virtual lanes.

14. (Currently Amended) A switch network according to claim 8 wherein said timing signal initiates ~~are reset~~ clearing of said plurality of storage registers.

15[[16]]. (Original) A switch network according to claim 8 wherein said card adaptor is a host channel adaptor.

16[[17]]. (Currently Amended) A switch network according to claim 15 ~~claim 16~~ wherein said host channel adaptor is an Infiniband host channel adaptor.

17[[18]]. (Original) A switch network according to claim 8 wherein said card adaptor is a target channel adaptor.

18[[19]]. (Currently Amended) A switch network according to claim 17 ~~claim 18~~ wherein said host channel adaptor is an Infiniband host channel adaptor.

19[[20]]. (Original) A switch network according to claim 8 further including a central processing unit for sending data to and receiving data from said memory device.

20[[21]]. (Currently Amended) A method for managing a buffer comprising a plurality of addressable memory registers, comprising:

partitioning the buffer into the plurality of buffer regions controlled by hardware;

monitoring, with the hardware, ~~the~~ usage of each buffer region within a time period; and

re-allocating the memory registers among the buffer regions with the hardware, based on the monitored usage.

21[[22]]. (Currently Amended) The method of claim 20 ~~claim 21~~, further comprising associating each buffer region with a data class.

22[[23]]. (Currently Amended) The method of claim 20 ~~claim 21~~, wherein at least one buffer region is associated with a data class representative of a virtual lane.

IN THE DRAWINGS:

The attached sheet of drawings includes changes to Figs. 1 and 2.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

This is intended as a full and complete response to the Office Action dated March 9, 2006, having a shortened statutory period for response set to expire on June 9, 2006. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-22 are pending in the application. Claims 1-22 remain pending following entry of this response. Claims 1, 5, 7, 8, 12, 14, 16, 18 and 20-22 have been amended. Applicant submits that the amendments do not introduce new matter.

Drawings

Figures 1 and 2 were objected to under MPEP § 608.02(g) as to lacking the designation of "Prior Art" because only that which is old is illustrated. Figures 1 and 2 have been corrected in compliance with 37 CFR 1.121(d) as requested by the Examiner. Further, the replacement sheets associated with these drawings have been labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures.

Accordingly, Applicant submits Figures 1 and 2 are in compliance with MPEP § 608.02(g) and requests withdrawal of this objection.

Specification

The abstract of the disclosure was objected to because all extraneous markings (particularly "Atty docket No. ...") should have been removed. The heading "Atty docket No. ..." is not part of the abstract, and should have been stripped off by the publication department. The published patent application currently bears no such heading.

As such, Applicant submits the specification is in compliance with MPEP § 608.01(b) and requests withdrawal of this objection.

Claim Objections

Claims 16-23 were objected to because they should have been renumbered 15-22. These claims have been renumbered in compliance with the Examiner's objections.

Claims 1 and 8 were objected to because of spelling errors of the words "partitioning" and "re-partitions". These claims have been corrected in compliance with the Examiner's objections.

Claims 5 and 12 were objected to because of the uses of the phrases "the least used buffer" and "the minimum number of addressable", recited on lines 1 and 2 respectively. These claims have been corrected in compliance with the Examiner's objections.

Claim 20 was objected to because of the use of the phrase "the usage" recited on line 5. This claim has been corrected in compliance with the Examiner's objections.

Accordingly, Applicant respectfully requests withdrawal of these objections.

Claim Rejections - 35 U.S.C. § 112

Claims 7 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

Claim 7 has been rephrased, as suggested by the Examiner on page 3 of the Office Action, to correct a typographical error. Claims 7 and 14 have been amended to

recite "clearing" of counter registers, which is supported in the specification (e..g, see paragraphs [0012] and [0025].

Accordingly, Applicant submits claims 7 and 14 are in compliance with the enablement requirement and request withdrawal of this rejection.

Claim Rejections - 35 U.S.C. § 102

Claims 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Muller (US Patent 6,044,418).

Applicant respectfully traverses this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, Muller does not disclose "each and every element as set forth in the claim". For example, Muller does not disclose the reallocation of memory registers among the buffer regions with hardware, as recited in claim 20. The Examiner argues that Muller discloses the reallocation of the buffer memory registers using hardware, since the hardware is used for monitoring (page 5, lines 10-12). However, even the Examiner himself concedes that it is the software that is performing the actual reallocation (page 5, lines 12-14).

Claim 20 recites that the reallocation of the memory registers among the buffer regions is to be done with hardware, and in fact never mentions the use of software ("re-allocating the memory registers among the buffer regions with the hardware, based on

the monitored usage"). Muller, on the other hand, provides that it is the software which functions "to dynamically reallocate the sizing of partitions according to usage" (column 2, lines 9-10). Muller uses "programmable partition pointers" which determine "how the partition boundaries are to be moved" (column 5, lines 26-28), and "software... to determine when the partitioning process is complete" (column 5, lines 32-34).

Accordingly, Applicant submits that claim 20 and its dependants, including claim 21, are allowable. Applicant requests, therefore, that the rejection of these claims be withdrawn.

Claim Rejections - 35 U.S.C. § 103

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller (US Patent 6,044,418) as applied to claim 20 above, and in further view Gil (US PG Publication 2004/0064664 A 1). Claim 22 depends upon claim 20, which Applicant submits is allowable for the reasons discussed above. Accordingly, Applicant submits this claim is allowable and requests withdrawal of this rejection.

Claims 1-5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller (US Patent 6,044,418) in view of Welch et al. (US Patent 6,735,633 B1).

Claims 6 and 8-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Muller (US Patent 6,044,418), Welch (US Patent 6,735,633 B1) and Mammen (US PG Publication 2004/0047367 A1), and in further view of Gil (US PG Publication 2004/0064664 A 1).

Applicant respectfully traverses these rejections.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill

in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejections fail to establish at least the third criterion.

For example, the references, even when combined as suggested in the Office Action, fail to teach the use of a logic network write and read data from a plurality of data classes into a plurality of buffer regions such that each data class is written into and read from a different buffer region, as recited in independent claims 1 and 8.

The use of reading and writing data classes into different buffer regions, as recited in the claims, allows a buffer memory to store the data associated with each network in its own portion of the data buffer memory space. In contrast, Muller teaches no such use of reading and writing data classes into different buffer regions, but rather only teaches the use of queues maintaining pointers to buffers containing data, or in the alternative, queues containing the data itself, without the assignment of each network's data to a corresponding and separate data class (see page 6, lines 26-31). Likewise, neither Welch nor Mammen address the assignment of each network's data to a corresponding and separate data class, as recited in the claims. In fact, neither reference mentions the use of different data classes whatsoever.

Accordingly, Applicant submits that claims 1 and 8, as well as their dependants, are allowable and withdrawal of this rejection is respectfully requested.

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the office action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted,

Randol W. Read
Registration No. 43,876
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)

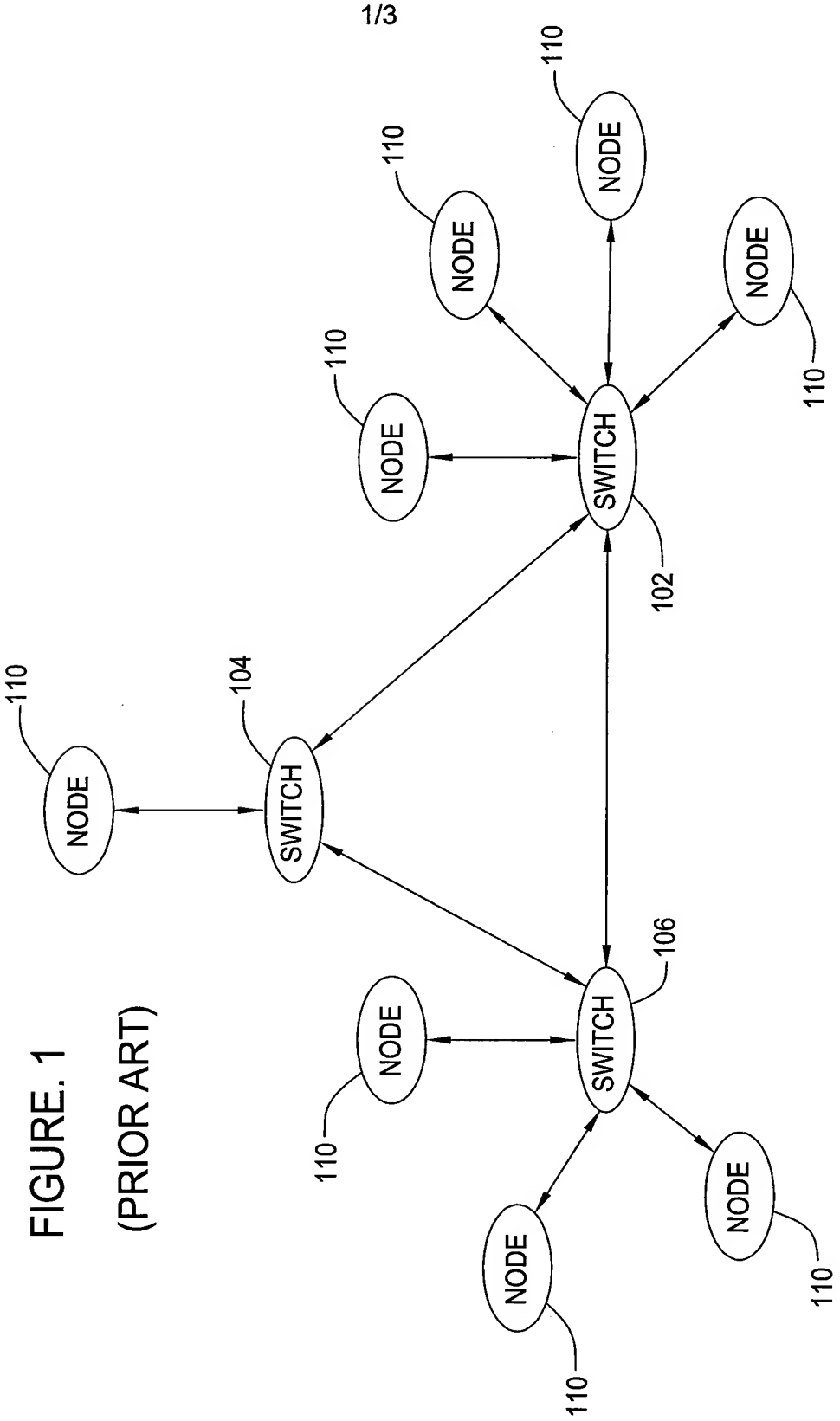

FIGURE. 1
(PRIOR ART)

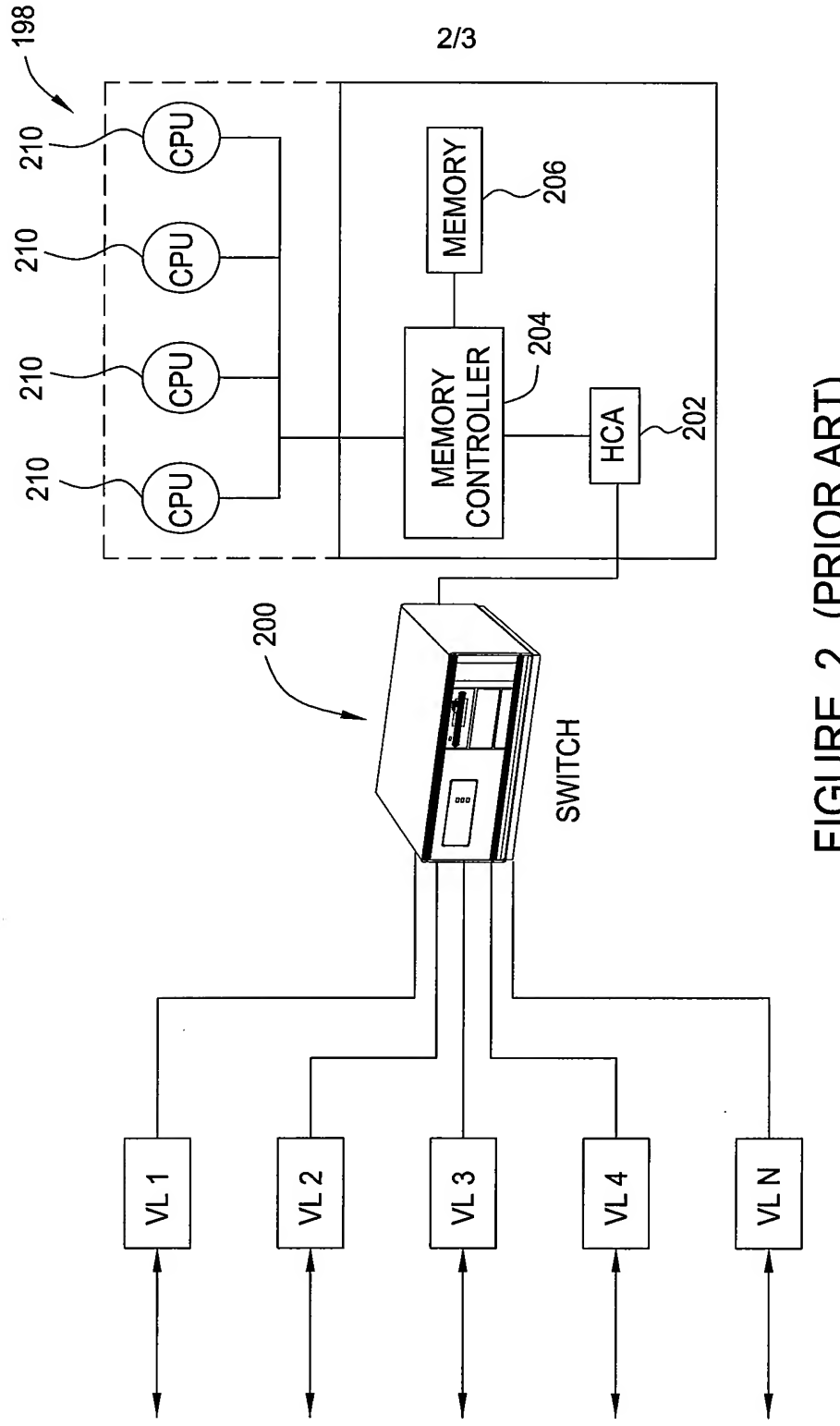

FIGURE. 2 (PRIOR ART)

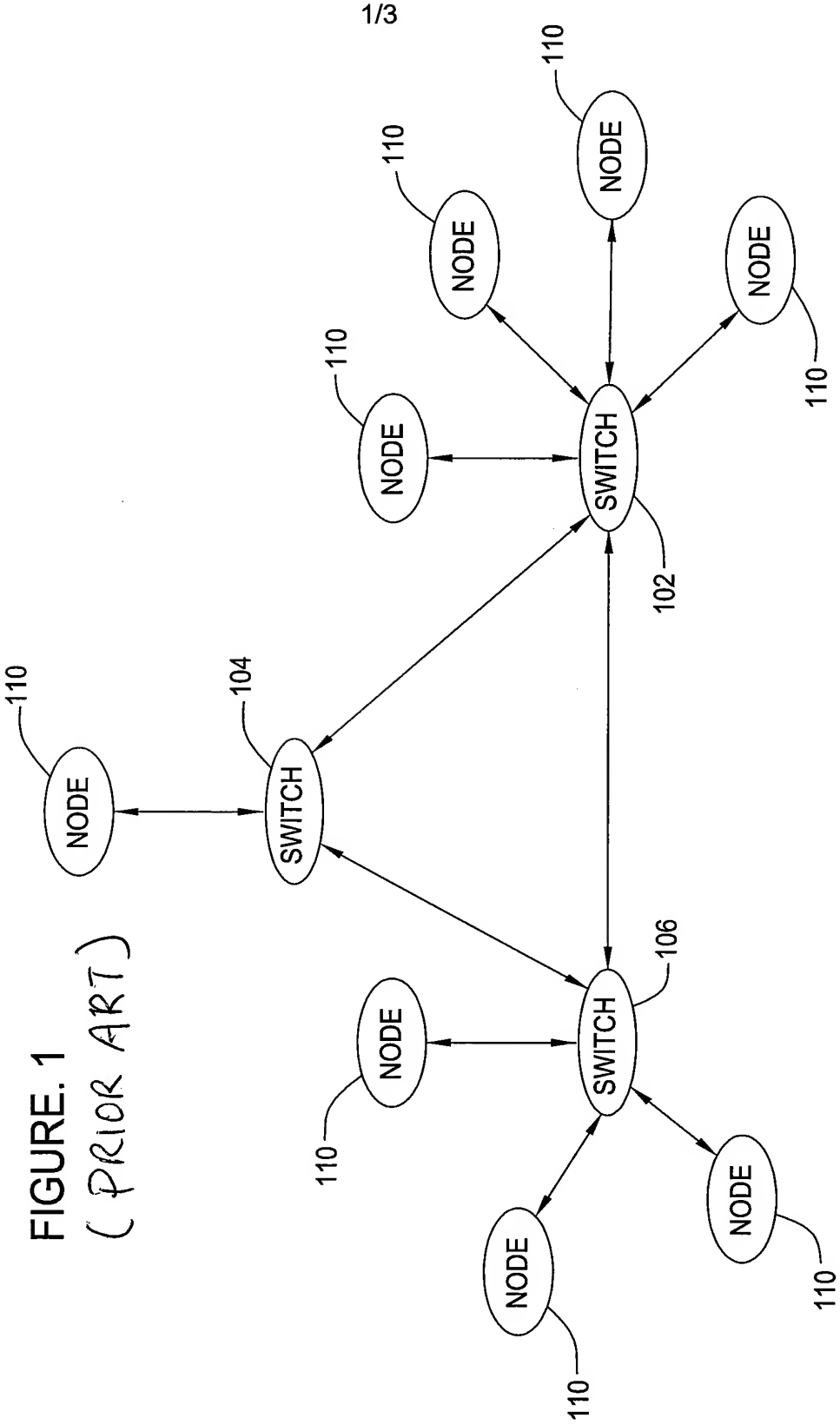

FIGURE. 1
(PRIOR ART)

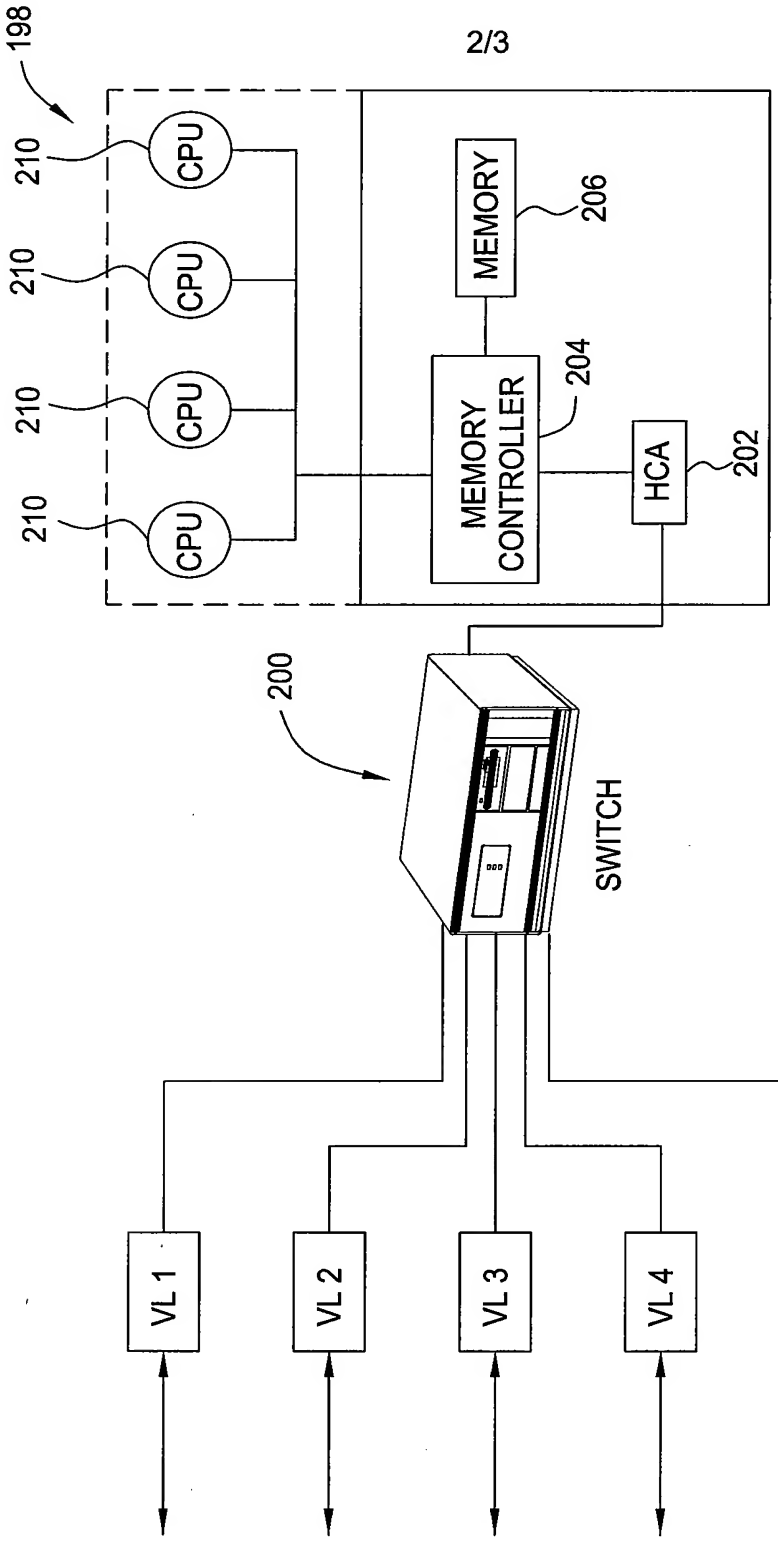

FIGURE. 2 (PRIOR ART)